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Specification of FUJITSU TFT-LCD module

NA19026-C661

	Approval	
Date :		
Ву:		

This Product is designed, developed and manufactured as contemplated for general use, including without limitation, general office use, personal use, household use, and ordinary industrial use, but is not designed, developed and manufactured as contemplated for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could lead directly to death, personal injury, severe physical damage or other loss (hereinafter "High Safety Required Use"), including without limitation, nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system. If customer's product possibly falls under the category of High Safety Required Use, please consult with our sales representatives in charge before such use. In addition, FDTC shall not be liable against the customer and/or any third party for any claims or damages arising in connection with the High Safety Required Use of the Product without permission.

Specification No.: Tech Bes LCD-00288

Issue Date : September 8, 2004

Issued by:

K. Tanaka **Project Director**

LCD Product Div.

FUJITSU DISPLAY TECHNOLOGIES CORPORATION

Global LCD Panel Exchange Center

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TABLE OF CONTENTS 2. PRODUCT NAME AND MODEL NUMBER 4. CONFIGURATION ______2 6. ABSOLUTE MAXIMUM RATING...... 4 7. RECOMENNED OPERATING CONDITION...... 4 8. ELECTRICAL SPECIFICATIONS 5 10. INTERFACE SPECIFICATION С **BACKLIGHT SPECIFICATION** ENVIRONMENTAL SPECIFICATION......24 **12**. 13. PACKAGING SPECIFICATION......25 14. 15. 16. 17. DOCUMENT CONTROL SECTION RETURN METHOD FOR PRODUCT REPAIR • COMPLAINT....... 31 18 OUTLINE DRAWING......35 Ε TITLE NA19026-C661 DRAW. NO. CUST. Tech Bes LCD-00288

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6. ABSOLUTE MAXIMUM RATING

Table 6-1 shows the absolute maximum rating of this LCD module.

Table 6-1 Absolute Maximum Rating

Item	Symbol	Condition	MIN.	TYP.	MAX.	UNIT
Supply Voltage (3.3V)	Vcc	Ta=25℃	-0.3		4.0	V
Supply Voltage (EDID)	VEDID		-0.3	_	6.25	V
Input Signal Voltage (LVDS)	VIN		-0.3	_	Vcc+0.3	V
Input Signal Voltage (EDID)	VINED		-0.3		Vedid +0.3	V

7. RECOMMENDED OPERATIONG CONDITIONS

Table 7-1 shows the recommended operating conditions

Table 7-1 Recommended Operating Conditions

Item	Symbol	MIN.	TYP.	MAX.	UNIT
Supply Voltage (3.3V)	Vcc	3.0	3.3	3.6	V
Supply Voltage (EDID)	V _{EDID}	2.7	_	5.5	V
Ripple Voltage (V CC)	V RP		_	100	mVp-p

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8. ELECTRICAL SPECIFICATIONS

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Table 8-1 shows the electrical specifications of this LCD module. Figure 8-1 shows the measurement circuit. Figure 8-2 shows the equivalent circuit of the logic signal input area.

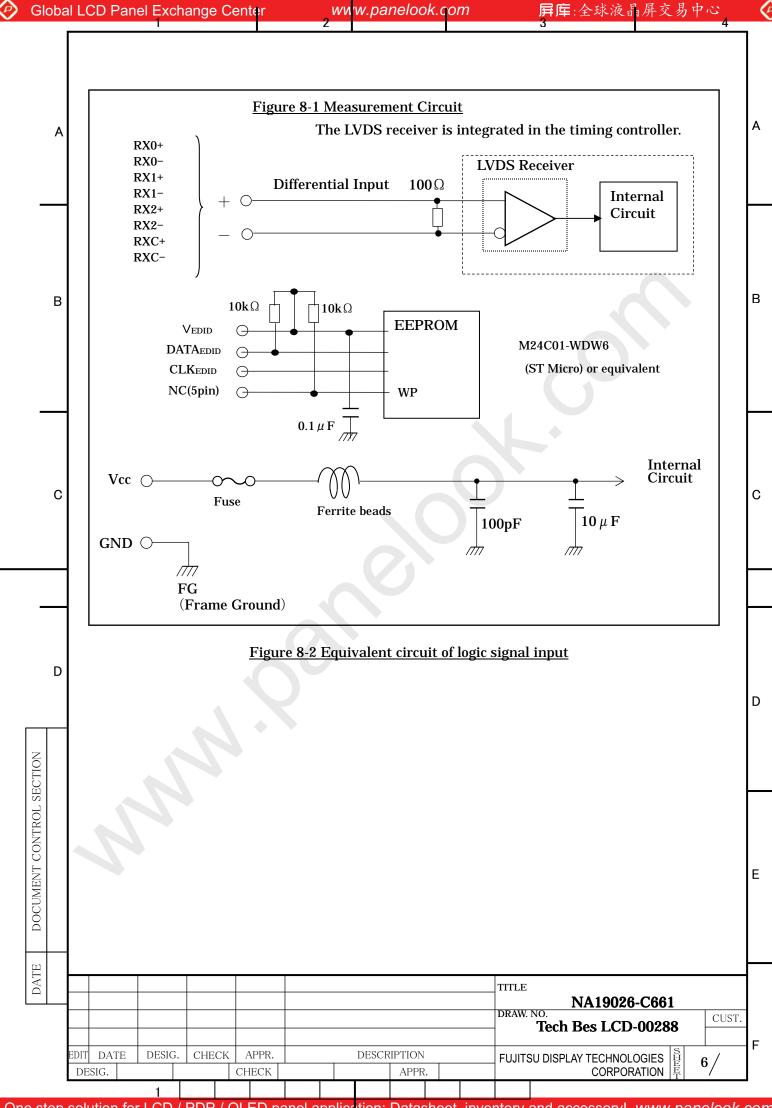
Table 8-1 Electrical Specifications

	Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Dif (+)	ferential input Voltage	VIH	V cm=+1.2V	_	_	100	mV
Dif (-)	ferential input Voltage	VIL	V CIII—+1.2V	-100		_	mV
Suj	oply Current	I cc	VCC=+3.3V VSS=0V		560	850	mA
Suj	oply Rush Current	I scc	Ta=25°C CK=54.0MHz			2.5	A
	oply Rush Current ration (excess 1.2A)	Tscc	Frame frequency =60Hz			2	ms
	CCFL Turn on Voltage (Note)	Vs	fL=50kHz,Ta=25°C, C _L =22pF		1	1650	Vrms
B,			fL=50kHz,Ta=0°C, C _L =22pF			1700	Vrms
BACK	Lighting Voltage	VL	fL=50kHz,IL=6mA		730	_	Vrms
LIGHT	Lighting Frequency	f L		40	60	80	kHz
HT TH	Recommended Lighting Frequency		VL=730Vrms,IL=6mA	50	_	60	kHz
	FL tube Current (Note2)	lι	VL=730Vrms fL=50kHz	2	6	6.5	mA

Note) The CCFL turn on voltage is set under the appointed criteria and shall exceed the maximum range of the specification.

●Measurement circuit is based on Figure 8-1

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9.. OPTICAL SPECIFICATIONS

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Table 9-1 shows the optical specifications of this LCD module.

Table 9-1 Optical Specifications

	Table of Optical C									
	7.	G 1.1		1	S	pecificati	on	TT	D 1	NT 4
	Item	Symbol	Cond	dition	MIN.	TYP.	MAX.	Unit	Remark	Note
	Visual Angle	$ heta_{ ext{L,R}}$	CR≧10 Ta=25	θ _{U,D} = 0°	80			deg	Top Bottom	(1)(2) (3)(5)
		$oldsymbol{ heta}_{ ext{U,D}}$	℃	θ _{L,R} = 0°	80	_		deg	Left Right	(6)
В	Contrast Ratio	CR	θ _{L,R,U,D} = Ta=25°C		250	400	_	_	White / Black*1	(1)(3) (5)
	Response Time (ON)	t on	$\theta H=0^{\circ}$ $\theta V=0^{\circ}$	Ta=25 ℃	_	15	30	ms		(1)(4) (5)
	(B→W)			Ta=0°C	_	50	100	ms		
\dashv	Response time	t off	θ H=0°	Ta=25 ℃	_	10	25	ms		
	(OFF) (W→B)		θ v=0°	Ta=0°C	_	50	100	ms		
С	Brightness	L			190	300) —	cd/m²	All white	(1)(5)
	Brightness Uniformity	ΔL	$\theta H=0^{\circ}$ $\theta V=0^{\circ}$		60		_	%	display *2,3,4	(1)(7)
_	Chromaticity (White)	х	Ta=25℃ fL=50kH	z	0.283	0.313	0.343	_		(1)(5)
		У	If=6mA		0.299	0.329	0.359	_		
	Color Purity (NTSC ratio)				55	63		%		(1)(5)
	LCD Panel Typ	oe			TFT Co	olor				
D	Display Mode				Normal	lly Black				
	Wide Viewing	Angle Tech	nology		MVA					
	Optimum Viewing Angle			Symme	etry					
	Display Color				262,144	1 (6 bit co	lor)			
	Color of non-di	splay area	ļ		Black					
	Surface Treatm	nent			Glare Low ref	flection 2	2H			

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10. INTERFACE SPECIFICATIONS

10.1 Interface Signal Alignment

Table 10-1 shows the description and configuration of the interface signals (CN1)

Table 10-1 Interface signals

	Table 10 1 Intel	
Pin No.	Symbol	Function
1	VCC	+3.3V power supply
2	VCC	+3.3V power supply
3	VSS	Ground
4	VSS	Ground
5	RX0-	LVDS signal 0-
6	RX0+	LVDS signal 0+
7	VSS	Ground
8	RX1-	LVDS signal 1-
9	RX1+	LVDS signal 1+
10	VSS	Ground
11	RX2-	LVDS signal 2-
12	RX2+	LVDS signal 2+
13	VSS	Ground
14	RXC-	LVDS signal CLK-
15	RXC+	LVDS signal CLK+
16	VSS	Ground
17	VEDID	DDC+3.3Vpower supply
18	NC	NC
19	CLKEDID	DDC clock
20	DATAEDID	DDC data

Connector used : FI-SEB20P-HF13

Adapted Connector: FI-SE20M

Name of Maker : Japan Aviation Electronics Ltd.

Note) Terminal 18 should be open.

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Table	10-	<u>د ل ۵</u>	<u>v DS</u>	Data	HSSI	<u>timment</u>

	Input		ransmitter OS90C365	Interface	connect	or	LCD Control
Α	Signal *1	pin	INPUT	System side	LCI pin	D module	input
	R0	44	TxIN0			_	R0 R1
	R1 R2	45 47	TxIN1 TxIN2	Tx OUT0+	6	Rx0+	R2 R3
	R3	48	TxIN3				R4
	R4	1	TxIN4	Tx OUT0-	5	Rx0-	R5
	R5	3	TxIN5				G0
В	G0	4	TxIN6				
							C1
	G1	6	TxIN7				G1 G2
	G2 G3	7 9	TxIN8 TxIN9	Tx OUT1+	9	Rx1+	G2 G3
	G3 G4	10	TxIN9 TxIN10				G4
	G5	12	TxIN11				G5
	B0	13	TxIN12	Tx OUT1-	8	Rx1-	B0
	B1	15	TxIN13				B1
С							-
	B2	16	TxIN14				B2
	B3	18	TxIN15				B3
	B4	19	TxIN16	Tx OUT2+	12	Rx2+	B4
	B5	20	TxIN17				B5
	RSVD RSVD	22 23	TxIN18 TxIN19	T. OLITO	11	Rx2-	Not use
	ENAB	23	TxIN19	Tx OUT2-	11	KXZ-	Not use
	ENAD	23	IAIIVAU				ENAB
D			7				
				TxCLK OUT+	15	RxC+	
	DCLK	26	TxCLK IN				DCLK
				TxCLK OUT-	14	RxC-	

 $^{^{*}1}$ The RSVD (reserved) pin on the transmitter should be connected to the Ground

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10.2 CORRESPONDENCE BETWEEN COLOR AND INPUT SIGNAL

Table 10-3 shows the correspondence between input signal and color

Ι,			2 10-3	shows the co	rrespondence	between input signal an	a coloi
		or and			Data Sig	gnal (0:Low Level, 1:High	Level)
		ghtness					20101)
	Gra	adation		R5 R4 R3	R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0
		Black		0 0 0	0 0 0	0 0 0 0 0 0	0 0 0 0 0 0
1	ī	Blue		0 0 0	0 0 0	0 0 0 0 0 0	1 1 1 1 1 1
	Color	Green		0 0 0	0 0 0	1 1 1 1 1 1	0 0 0 0 0 0
	Ö	Cyan		0 0 0	0 0 0	1 1 1 1 1 1	1 1 1 1 1 1
	C	Red		1 1 1	1 1 1	0 0 0 0 0 0	0 0 0 0 0
	Basic	Magenta		1 1 1	1 1 1	0 0 0 0 0 0	1 1 1 1 1 1
	Щ	Yellow		1 1 1	1 1 1	1 1 1 1 1 1	0 0 0 0 0
		White		1 1 1	1 1 1	1 1 1 1 1 1	1 1 1 1 1 1
		Black	0	0 0 0	0 0 0	0 0 0 0 0 0	0 0 0 0 0 0
	J	仓	1	0 0 0	0 0 1	0 0 0 0 0 0	0 0 0 0 0 0
	tior	Darker	2	0 0 0	0 1 0	0 0 0 0 0 0	0 0 0 0 0 0
	Gradation	仓		::::	: : : :	::::::	:::::::
H	ra		:	::::	: : : :	:::::::	
		①	:	::::	: : : :	:::::::::::::::::::::::::::::::::::::::	
	Red	Brighter	61	1 1 1	1 0 1	0 0 0 0 0 0	0 0 0 0 0 0
	Н	①	62	1 1 1	1 1 0	0 0 0 0 0	0 0 0 0 0 0
		Red	63	1 1 1	1 1 1	0 0 0 0 0 0	0 0 0 0 0 0
		Black	0	0 0 0	0 0 0	0 0 0 0 0 0	0 0 0 0 0 0
	uo	仓	1	0 0 0	0 0 0	0 0 0 0 0 1	0 0 0 0 0 0
	Gradation	Darker	2	0 0 0	0 0 0	0 0 0 0 1 0	0 0 0 0 0 0
	ad	仓		::::	: : : :	:::::::	:::::::
┨	Gr		:	::::	::::	1::::::	
	Э'n	Ω	:	::::	: : : :		
┨	Green	Brighter	61	0 0 0	0 0 0	1 1 1 1 0 1	0 0 0 0 0 0
	9	Û	62	0 0 0	0 0 0	1 1 1 1 1 0	0 0 0 0 0 0
П		Green	63	0 0 0	0 0 0	1 1 1 1 1 1	0 0 0 0 0 0
		Black	0	0 0 0	0 0 0	0 0 0 0 0 0	0 0 0 0 0 0
	ion	矿	1	0 0 0	0 0 0	0 0 0 0 0 0	0 0 0 0 0 1
	atic	Darker	2	0 0 0	0 0 0	0 0 0 0 0 0	0 0 0 0 1 0
	Gradat	仓		: : : :	: : : :		
1	Gra	_			: : : :		
		Û			: : : :		
	Blue	Brighter	61	0 0 0	0 0 0	0 0 0 0 0 0	1 1 1 1 0 1
		Û	62	0 0 0	0 0 0	0 0 0 0 0 0	1 1 1 1 1 0
		Blue	63	0 0 0	0 0 0	0 0 0 0 0 0	1 1 1 1 1 1
ı							

Note 1) Definition of gray scale: Color (n)..."n" indicates the gray scale level.

The larger number means brighter level.

Note 2) Data: 1:High level, 0:Low level

Note 3) There are 18 color data which consists of 6 bit of red, green and blue where they individually display 64 signals. By combining these colors, 262,144 colors can be displayed.

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10.3 INPUT SIGNAL TIMING

The input signal timing is shown in table 10-3 and figure 10-1.

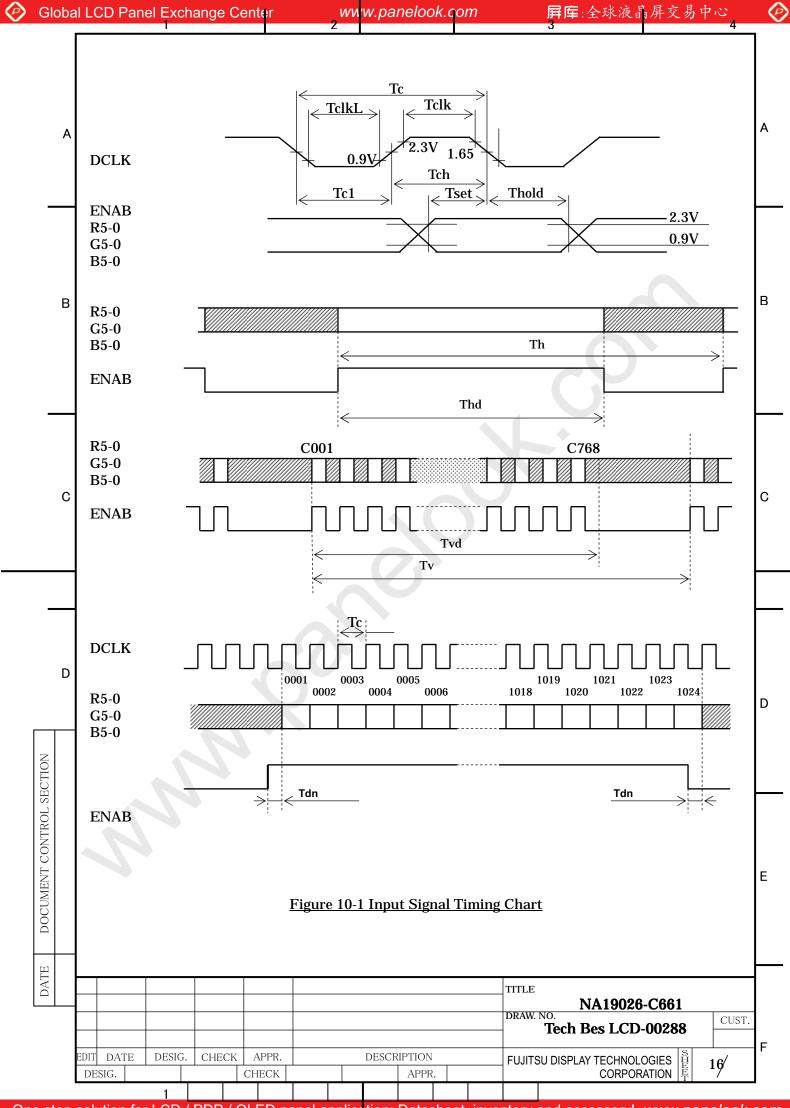
<u>Table 10-3 Timing Characteristics</u>

 $(Ta=0\sim50^{\circ}C, Vcc=3.3\pm0.3 V)$

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	Item	Symbol	MIN.	TYP.	MAX.	Unit	Remark
DCLK Signal (Clock)	Period Frequency Duty High time Low time	Tc 1/Tc Tch/Tc TclkH TclkL	15.15 60 45 6.0 6.0	15.38 65 50 —	16.67 66 55 —	ns MHz % ns ns	*4
DCLK-Data Timing	Setup time Hold time	Tset Thold	3 5	_ _	_ _	ns ns	
Horizontal Signal	Horizontal period Hor. Period (1) Hor. Display period	Th Th Thd	1320 18.0 1024	1344 20.68 1024	2046 — 1024	DCL K μs DCL K	*1,4 *4 *2
Vertical Signal	Vertical Period Ver. Frequency Ver. Display period	Tv 1/Tv Tvd	780 55 768	806 60 768	1023 65 768	Th Hz Th	*1 16.67ms *2
ENAB signal	Data ENAB timing	Tdn		0	_	DCL K	*3

- *1) • The horizontal direction of the display position is defined by the rise of the ENAB signal. Right after the signal rises, the latched data is displayed from the left edge of the screen. The vertical direction of the display position is when the ENAB signal changes from "H" to "L" and "L" is over 2048 DCLK, then the next risen ENAB signal data is displayed from the top line of the screen.
- If the "H" period of the ENAB signal is less then 1024 DCLK, then black is displayed on the *2) remaining area.
 - If the ENAB signal is less than 768 Th within a frame, then the displayed data is continuously displayed from the top line of the screen continuously.
- *3) If the valid data period and the "H" period of the ENAB signal do not synchronize, then the display position is displayed as out of place.
- When the horizontal period is less than 1320 DCLK or 18 μ s, the display quality such as unevenness and light line defect can occur. If the DCLK frequency exceeds 66MHz, garbled data may cause flickering. In addition, if the DCLK frequency is less than 60MHz, then unevenness may occur.



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10.6 EDID Signal Timing

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Table 10-4 shows DC characteristics of EDID signals. Figure 10-4 shows input timing. Table 10-5 shows AC characteristics and Table 10-6 shows the contents of EDID data.

> Table 10-4 EDID DC Characteristics $(Ta=0\sim50^{\circ}C, Vcc=3.3\pm0.3V)$

	Item	Symbol	MIN.	MAX.	Unit	Remarks
SCL,SDA Terminal	High voltage	VIH	0.7V _{EDID}	_	V	
input voltage	Low voltage	VIL	VIL — 0.3V _{EDID}		V	
Hysteresis	voltage	VHYS	0.05VEDID		V	
Output vo	ltage	VOL1 VOL2	_ _	0.4 0.6	V V	$\begin{array}{l} I0L{=}3mA,\ V_{\rm EDID}={2.5V}\\ I0L{=}6mA,\ V_{\rm EDID}={2.5V} \end{array}$
Input leak current	All input-and-output pins WP pin	Tv 1/Tv	-10 -10	10 50	μ A μ A	VIN=0.1V to V _{EDID} ,WP=VSS WP= V _{EDID}
Output lea	ak current	Tdn	-10	10	μΑ	VOUT=0.1V to Vedid
Terminal ca (Input and				p F	VCC=5.0V Ta=25°C, Fclk=1MHz	
Operating	current	ICC Wr ICC Re	7	3 1	m A m A	V _{EDID} =5.5V,SCL=400KHz V _{EDID} =5.5V,SCL=400KHz
Stillness c	illness current ICCS = 30 100		μ A μ A	VCC=3.0V,SDA=SCL=VCC VCC=5.5V,SDA=SCL=VCC WP=VSS,A0,A1,A2=VSS		

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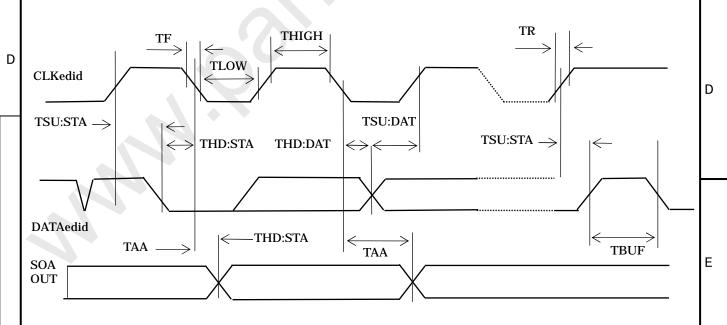
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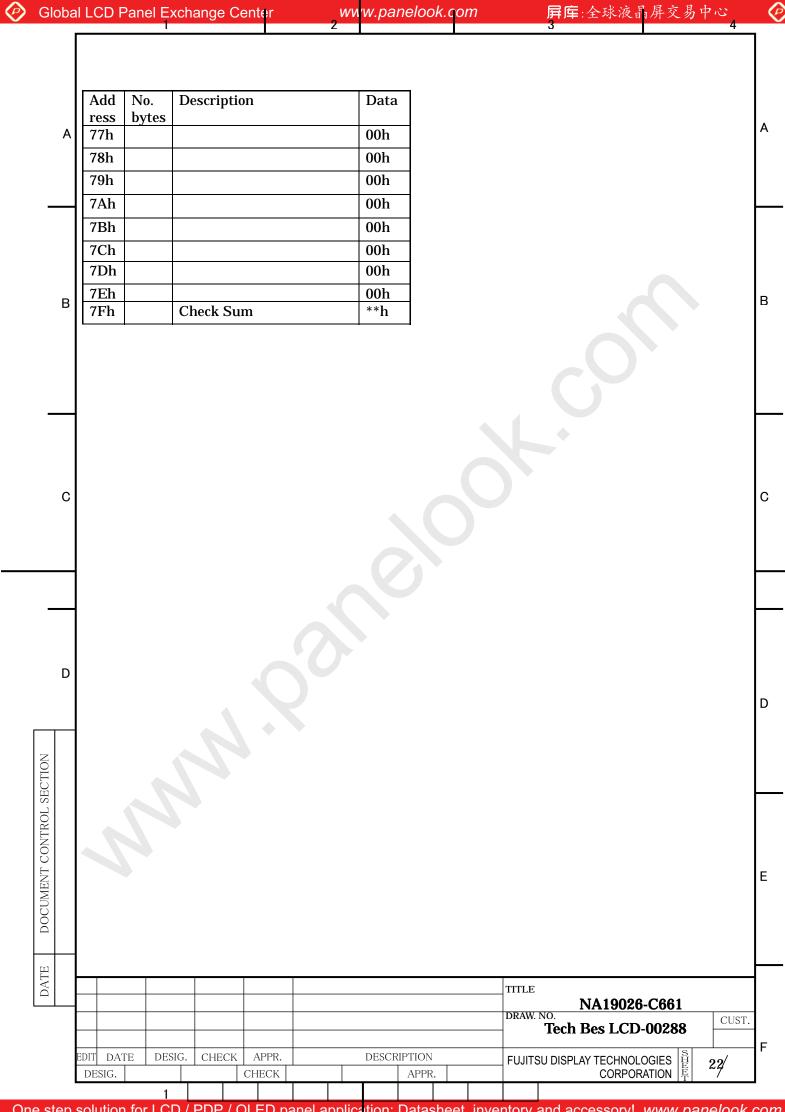
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Item	Symbol	Vcc=2.5 Stan operation	dard	Vcc=4.5 High-spec	ed	Unit	Remarks
		MIN.	MAX.	MIN.	MAX.		
Clock frequency	Fclk	_	100	_	400	kHz	
Clock high time	THIGH	4000		600		ns	
Clock low time	TLOW	4700		1300		ns	
SDA, SCL rising time	TR		1000	_	300	ns	
SDA, SCL falling time	TF	_	300	_	300	ns	
START hold time	THD:SDA	4000		600		ns	
START setup time	TSU:STA	4700		600		ns	
DATA input hold time	THD:DAT	0	_	0	_	ns	
DATA input setup time	STU:DAT	250	_	100	-(ns	
STOP setup time	TSU:STO	4700	_	600		ns	
Output decision time from a clock	TAA	100	3500	100	900	ns	
Bus free time	TBUF	4700	_	1300	_	ns	
Minimum VIH, VIL Rising time	TOF		250	20+0.1CB	250	ns	CB≦100pF
Spike oppression (SDA, SCL pins)	TSP		50		50	ns	
A write-in cycle time	TWR	-	10		10	ms	Byte and page mode
The number of times of data rewriting	_	1M		1M		cycle	25°C,Vcc=5.0V block mode





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11 BACK-LIGHT SPECIFICATION

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11-1 Pin configuration for Back-light

Table 11-1 shows the description of the pin assignment and the types of back-light (CN-2)

Table11-1 Pin Assignment of CN-2

Pin No.	Signal	Function	Remark
1	Vн	Power supply for CCFL (High)	Cable color: Pink
2	V L	Power supply for CCFL (Low)	Cable color: White

BHSR-02VS-1Used connector : Applied connector : SM02B-BHSS-1

Maker Japanese Solderless Terminal Trading Company LTD. (J.S.T)

11-2 Life

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The life duration of the LCD panel is considered to be over 50,000 hours.

The life duration of the Back Light is considered to be over 10,000 hours based on the criteria bellow.

(1)Operating condition

1 Ambient temperature 2 5 ± 5 °C

6 m A or less ②Tube current(IF) :

(2) Definition of life

- ① When brightness is bellow 50% of the minimum brightness value shown in section 9, table 9-1.
- ② When the CCFL turn on voltage stated in section 8 of table 8-1 exceeds 1700Vrms
- **3** When flickering and blinking occurs based under the condition of life guarantee.

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12. Environmental Specification

Table 12-1 shows the environmental specification.

Table 12-1 Environmental Specification

Item		Specification	Remark
Tomporaturo	Operation	0~50℃	The temperature of the LCD panel surface (display area)
Temperature	Storage	-20~60℃	temperature.
I Imiditer	Operation	20~85%RH	Maximum wet bulb temperature Should not exceed 29℃.
Humidity	Storage	5~85%RH	No condensation
Vibration	Operation	10-500Hz, 2G peak, 2 Hrs each in X,Y,Z direction Approx. 20 min for 1 cycle.	For single module. Test criteria is stated in (Note 1)
Shock	Non- operating	15G, 6ms, 1 time each for X,Y,Z direction	For single module. When packaging refer to (Note 2)

Note 1) The distance between the vibration table and the back surface of the LCD module should be set to 3mm when conducting a vibration test. Note 2) The shock resisting standard when packing is shown in table 12-2 and

figure 12-1.

Table 12-2 Shock resistance standard when packaging module

No. of times	Dropping height	oint	Contact po	
1 time each	5 5 c m		B, C, D	Α,
i time each	6 0 c m	I, J	F, G, H,	Ε,

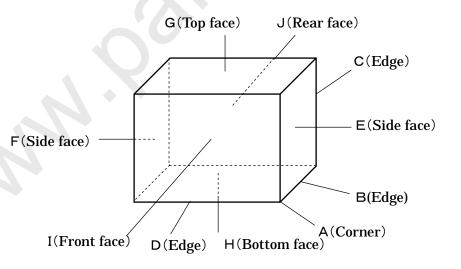


Figure 12-1 The direction of applying shock when packing

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1 6. PRECAUTIONS

In order to use the LCD module properly, please abide by the following precautions.

(1)Handling of LCD panel

① Do not apply excessive mechanical shock to the LCD panel

The panel is made of glass. Excessive shock may cause damage or malfunction to the LCD panel.

② Do not press the panel surface too hard (MAX 20N/cm²)

There are 2 glass plates within the panel and they should be kept perfectly even to maintain display properties and reliability. If the panel is pressed hard, then the following problems may occur;

1 Color uniformity 2Disorder of orientation of liquid crystal

Problem ① will clear as time passes. For problem ②, turn the power off and then on in order to bring the screen back to normal. However, these operations should be avoided to insure reliability.

3Do not scratch the polarizer film on the LCD panel surface

- Do not press or rub the display surface with a hard tool, tweezers, etc.
- When handling the panel, use cotton or conductive gloves so that the display surface is not soiled.
- If dust or dirt soils the display surface, use a soft cloth (deer skin) to clear the panel using the following method;

[Dust] Dust the panel using a soft cloth. (Do not rub).

- [Dirt] Saturate clear water to a soft cloth and squeeze hard until there are no water drops, then wipe the surface lightly. Make sure water or solvents are not splashed onto the edge of the panel to prevent fluid from seeping into the panel. Do not use alcohol, detergent, ketone (acetone, etc.) and aromatics (xylene, tolune, etc.) as solvents.
- Adherence of saliva and water drops for a long period may cause partial deformation and decolorization. Clean the surface promptly using the [Dirt] method.
- Cleaners that are alkaline will damage the surface of the polarizor and should not be
- Adherence of excessive oil is hard to clean and precaution should be taken to avoid oil adherence.

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has been turned on

contrast ratio etc.

reliability.

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DOCUMENT CONTROL SECTION

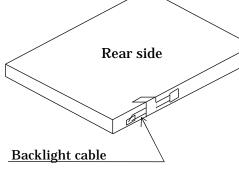
18. Return method for LCD module when requested for repair or analysis of the problem

When returning the LCD module, follow the procedure accordingly by not damaging the LCD panel or the backlight cables. (Refer to Figure 18-1,2,3,4)

It should be noted that FDTC would not take responsibility for damaged LCD modules that are returned where the reason for damage is due to failure of following the specified packaging procedure.

18-1 In case of made in Taiwan

(1) Stabilize the back light cable using tape.



If the cables are not stabilized, the connectors may scratch the LCD panel surface or it can cause damage to the cables. Α

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(2) Put the LCD module into the anti-electrostatic bag. (Do not use anti-electrostatic bag that are torn)

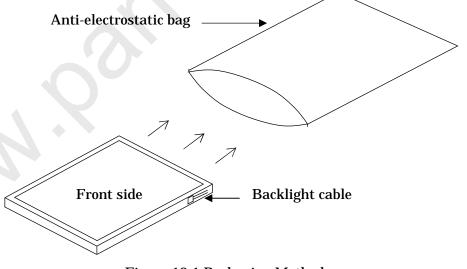


Figure 18-1 Packaging Method

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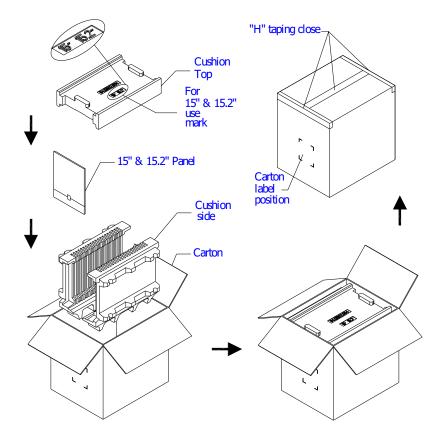
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- - When using a carton box manufactured by FDTC (Carton boxes and arrowheads that are not crushed should be used)

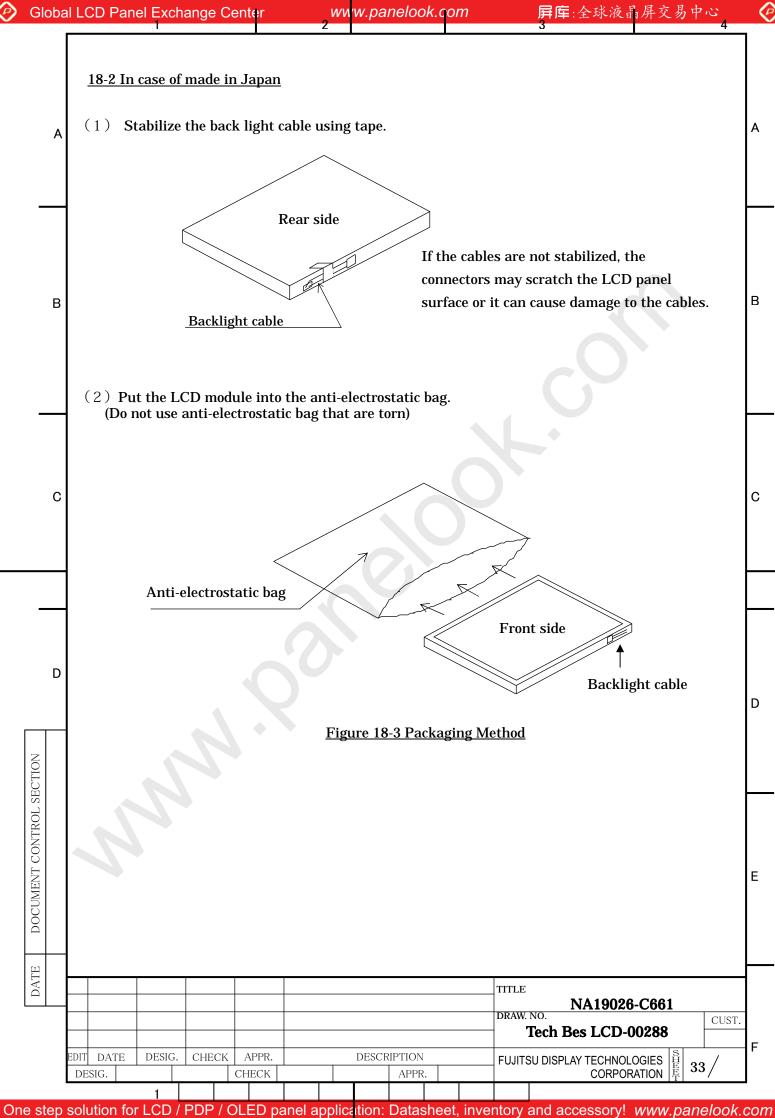


Place the front side of the LCD module in the direction of the arrow shown on the holder (top).

****Directions of arrowheads are shown on holders****

Figure 18-2 Packaging Method

When using other methods of packaging other than specified above Thoughtful consideration should be taken so that damage is not made to the LCD module by wrapping the module individually with an air cap. It should be noted that FDTC would not take responsibility for damages caused by failure of packaging



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